AMENDMENTS TO THE CLAIMS

Following is a listing of all claims in the present application, which listing supersedes all previously presented claims:

Listing of the claims:

1. (Currently Amended) A PLL frequency synthesizer, comprising:

a voltage-controlled oscillator for outputting an output frequency signal corresponding to a control voltage signal;

a phase comparator for outputting an output signal corresponding to a phase comparison between the output frequency signal and a reference frequency signal; and

a charge pump circuit for varying the control voltage signal according to the phase-compared signal;

whereby a feedback loop in a locked state is configured,

wherein signal flow of the feedback loop is periodically varied in a predetermined period, the predetermined period including the timing of performing an operation of phase comparison between the output frequency signal and the reference signal in the phase comparator ~~an output period of the reference frequency signal subjected to comparison in a phase comparison cycle of the phase comparator~~.

2. (Currently Amended) The PLL frequency synthesizer according to claim 1, wherein the operation of the feedback loop periodically stops in a ~~the~~ phase comparison cycle used in the phase comparator.

3. (Original) The PLL frequency synthesizer according to claim 2, wherein the feedback loop includes a loop opening/closing switch circuit therewithin.

4. (Original) The PLL frequency synthesizer according to claim 3, wherein a first filter circuit and a second filter circuit for determining the signal flow of the feedback loop are provided in a path which extends from the charge pump circuit to the voltage-controlled oscillator, and

the loop opening/closing switch circuit is provided between the first filter circuit and the second filter circuit.

5. (Original) The PLL frequency synthesizer according to claim 3, wherein the loop opening/closing switch circuit includes an MOS transistor.

6. (Original) The PLL frequency synthesizer according to claim 3, wherein the loop opening/closing switch circuit includes a JFET transistor.

7. (Original) The PLL frequency synthesizer according to claim 2, wherein the feedback loop stops the output of an output signal from the charge pump circuit.

8. (Original) The PLL frequency synthesizer according to claim 7, wherein the charge pump circuit includes a path opening/closing switch circuit in an output path for an output signal outputted from the charge pump circuit.

9. (Original) The PLL frequency synthesizer according to claim 8, wherein the path opening/closing switch circuit includes an MOS transistor.

10. (Original) The PLL frequency synthesizer according to claim 8, wherein the path opening/closing switch circuit includes a JFET transistor.

11. (Currently Amended) The PLL frequency synthesizer according to claim 1, wherein at least one filter circuit for determining the signal flow of the feedback loop is provided in a path which extends from the charge pump circuit to the voltage-controlled oscillator, and

the filter characteristic of the filter circuit is periodically varied in a ~~the~~ phase comparison cycle of the phase comparator.

12. (Original) The PLL frequency synthesizer according to claim 11, wherein the filter circuit includes,

a bypass path group having at least two bypass paths different in filter characteristic, and

a selector switch circuit which selects a predetermined bypass path from the bypass path group.

13. (Original) The PLL frequency synthesizer according to claim 12, wherein the bypass path group includes,

at least two filter constituent elements connected in parallel, and

the selector switch circuit which selectively switch at least one of the filter constituent elements as a constituent part of the predetermined bypass path.

14. (Original) The PLL frequency synthesizer according to claim 12, wherein the bypass path group includes,

at least two filter constituent elements connected in series, and

the selector switch circuit which selects at least one of the filter constituent elements by short-circuiting.

15. (Original) The PLL frequency synthesizer according to claim 12, wherein the selector which circuit includes a MOS transistor.

16. (Original) The PLL frequency synthesizer according to claim 12, wherein the selector switch circuit includes a JFET transistor.

17. (Original) The PLL frequency synthesizer according to claim 11, wherein the filter circuit includes a variable filter constituent element for varying the filter characteristic thereof.

18. (Original) The PLL frequency synthesizer according to claim 17, wherein the variable filter constituent element is an active resistive elemental device.

19. (Original) The PLL frequency synthesizer according to claim 18, wherein the active resistive elemental device is a MOS transistor.

20. (Original) The PLL frequency synthesizer according to claim 18, wherein the active resistive elemental device is a JFET transistor.

21. (Original) The PLL frequency synthesizer according to claim 1, wherein the charge pump circuit includes an output capability switching circuit for selecting the capability of supply of an output signal outputted from the charge pump circuit.

22. (Original) The PLL frequency synthesizer according to claim 21, wherein the output capability switching circuit selects a drive power source voltage for an output-stage circuit of the charge pump circuit.

23. (Original) The PLL frequency synthesizer according to claim 21, wherein the output capability switching circuit selects a drive current for an output-stage circuit of the charge pump circuit.

24. (Original) The PLL frequency synthesizer according to claim 21, wherein the output capability switching circuit selects an output transistor size for an output-stage circuit of the charge pump circuit.

25. (Currently Amended) The PLL frequency synthesizer according to claim 1, wherein a period in which the characteristic variation or the operation stop is performed~~, is a predetermined period which~~ includes an output period of the reference frequency signal subjected to comparison in the phase comparator.

26. (Original) The PLL frequency synthesizer according to claim 25, further including a frequency divider for frequency-dividing the reference frequency signal, and

wherein a frequency signal compared in the phase comparator is a divided frequency signal outputted from the frequency divider.

27. (Original) The PLL frequency synthesizer according to claim 4, wherein the filter circuit is either a voltage-driven type or a current-driven type.

28. (Original) The PLL frequency synthesizer according to claim 11, wherein the filter circuit is either a voltage-driven type or a current-driven type.